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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YALEW, FIKREMARIAM A	
ART UNIT	**PAPER NUMBER**
2136	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,321	ROBINSON ET AL.	
	Examiner	Art Unit	
	Fikremariam Yalew	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/12/2004,07/11/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 have been examined.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-33 are rejected under 35 U.S.C. 102(b) as being anticipated by EP 1,126,356(Kabushiki Kaisha Toshiba Aug 22,2001).

4. As per claim 1: Hashimoto discloses a method/system/an article of manufacture for operating a data processing machine, comprising: a) applying by a processor an encoding process to private-state data, where the private-state data captures a state of the processor (See 0036(i.e., encryption/decryption unit being part of the processor (lines 2-5) and where the private-state data captures a state of the processor (lines 5-6)) and Fig 1 and 0067); b) writing, to a location in storage, said encoded private-state data (See 0036 lines 8-10), the location being one that is accessible to software that may be written for the processor(See 0094 lines 7-9); and c) recovering the private-state data

from the storage according to a decoding process that can undo the encoding process(See 0037 lines 1-5 and 0098 lines 1-3).

5. As per claim 2: Hashimoto discloses the method wherein the encoding process is to discourage an attempt at recovering the private-state data from the storage by a process other than the decoding process (See 0035-0037,0040).

6. As per claim 3: Hashimoto discloses the method wherein the encoding process is only strong enough to cause an author of the software to apply, in writing said software, a technique prescribed by a manufacturer of the processor for accessing the private-state data from storage rather than circumventing said technique (See 0035-0037,0040,0082).

7. As per claim 4: Hashimoto discloses the method wherein the private-state data refers to one of a) the content of an internal register of the processor that is not explicitly identified in an instruction manual for the processor that is intended for use by software developers (See Fig 1 step 2113 and 0036), and b) the content of an internal register of the processor that is explicitly identified in an instruction manual for the processor that is intended for use by software developers but is stored in one of a format and a location that is not explicitly identified in an instruction manual for the processor that is intended for use by software developers(See Fig 1 step 2113 and 0036).

8. As per claim 5: Hashimoto discloses the method the method wherein the private-state data is written to one of a) a publicly accessible location in a register file of the processor (See Fig 1 step 2101 and 0036) b) cache (See Fig 3 step 152), and c)memory(See Fig 1 step 2103).

9. As per claim 6: Hashimoto discloses wherein the encoding process is one in which the location of the written contents of a given internal register of the processor changes arbitrarily at least once, while repeating a)-b)(See 0038-0043).

9. As per claim 7: Hashimoto discloses the method wherein the encoding process is one in which a storage format of the written contents of a given internal register of the processor changes arbitrarily at least once between big-endian and little-endian, while repeating a)-b)(See 0038-0043).

10. As per claim 8: Hashimoto discloses the method wherein the encoding process is one in which a cipher is applied to the contents of a given internal register to produce an encoded value which is then written to the location in storage (See 0045).

11. As per claim 9: Hashimoto discloses the method further comprising storing the recovered state data in a private storage of the processor (See 0040,0091).

12. As per claim 10: Hashimoto discloses an article of manufacture comprising: a data processing machine having a private internal state (See 0036,0067), the internal state to change as the machine executes instructions provided to it as part of a program, wherein the machine is to encode data about the internal state and write the encoded state data to a location in a storage unit (See 0036), wherein the location is accessible by an instruction set architecture of the machine(See 0094).

13. As per claim 11: Hashimoto discloses the article of manufacture wherein the data processing machine is a processor that has a special read micro-operation, to be used when the processor is to recover said state data from the storage unit (0046,0040).

14. As per claim 12: Hashimoto discloses the article of manufacture wherein the processor further includes an internal cache and is to also write the encoded state data to a public location in the cache (See Fig 3 step 152 and 0120).

15. As per claim 13: Hashimoto discloses the article of manufacture wherein the processor is to recover the state data and write the recovered state data to a private location in the data processing machine (See 0037,0098).

16. As per claim 14: Hashimoto discloses the article of manufacture wherein the processor is to recover the state data and configure itself with the recovered state data in preparation for resuming execution of a suspended task (0037,0098, 0129).

17. As per claim 15: Hashimoto discloses the article of manufacture wherein the processor is one for which there is a manufacturer-defined instruction that, when executed by the processor, recovers the state data from the storage unit (See 0035-0037,0040,0082).

18. As per claim 16: Hashimoto discloses the article of manufacture wherein the data processing machine is a processor for which a special micro-operation is defined for accessing the encoded state data from the storage unit, and wherein the processor further comprises an address obfuscation unit to receive an address value associated with given state data of the processor, the address value having been derived from a dispatch of the special micro-operation, the obfuscation unit to provide an encoded, physical address value that points to the actual location in the storage unit where the given state data is stored(0036-0037,0098,0129).

19 As per claim 17: Hashimoto discloses the article of manufacture wherein the data

processing machine is a processor for which a hardware control signal is defined for accessing the encoded data from the storage unit, and wherein the processor further comprises an internal cache, a data conversion unit to receive a data value from the internal cache as a result of a cache hit derived from the hardware control signal, the conversion unit to decode the data value into actual state data of the processor(See Fig 3 step 152 and 0120).

19 As per claim 18: Hashimoto discloses a computer system comprising: a processor (See 0064 and Fig 1 steps 2101); and a main memory communicatively coupled to the processor and having public region designated to store the processor's private state data in encoded form (See 0065-0066 and Fig 1 steps 2101,2103).

20. As per claim 19: Hashimoto discloses wherein the processor encodes the private-state data prior to storing it to the public region (See 0036).

21. As per claim 20: Hashimoto discloses wherein the processor decodes a value read from the public region prior to using it (See 0037,0083).

21. As per claim 21: Hashimoto discloses the system wherein the processor further includes an internal storage unit in which a public region is designated to store a copy of said private-state data in encoded form (See Fig 3 step 152 and 0120).

22. As per claim 22: Hashimoto discloses the system wherein the internal storage unit is one of a cache and a register file (See Fig 3 step 152 and 0120).

23. As per claim 23: Hashimoto discloses the system wherein a private region is designated in the internal storage unit to store said private-state data in unencoded form(See 0036,0041).

24. As per claim 24: Hashimoto discloses the system further comprising a system chipset communicatively coupling the processor to the main memory (See Fig 1).

25. As per claim 25: Hashimoto discloses a method for operating a data processing machine, comprising: encoding private state data about a state of the machine(See 0036-0037); and writing, to a location in storage, the encoded private state data(0036-0037), the location being accessible to software that is running on the machine(0094).

26. As per claim 26: Hashimoto discloses the method of wherein the encoding comprises ciphering a value of the private data to yield said encoded private data(See 0035-0037,0040).

27. As per claim 27: Hashimoto discloses the method wherein the private data about the state of the machine is one of a register value and a value from the storage(See 0035-0037,0040).

28. As per claim 28: Hashimoto discloses the method wherein the encoding comprises address encoding to obfuscate an address value of the private data(see 0036).

29. As per claim 29: Hashimoto discloses the method further comprising: recovering the private data from the storage according to a decoding process(See 0037,0098).

30. As per claim 30: Hashimoto discloses wherein the recovering comprises: reading a plurality of values from memory See Fig 1 steps 115,152 and 0040-41); and combining the read plurality of values to form a single unencoded value of said private data(See Fig 1 steps 115,152 and 0040-41).

31. As per claim 31: Hashimoto discloses wherein the recovering comprises: reading

a plurality values from one or more discontiguous locations of memory(See Fig 1 steps 115,152 and 0040-41); combining the read plurality values to form a single value((See Fig 1 steps 115,152 and 0040-0041); and decoding the single value to form an unencoded value of said private data(See Fig 1 steps 115,152 and 0040-41).

32. As per claim 32: Hashimoto discloses the private data refers to one of a) the content of an internal register of the machine that is not explicitly identified in an instruction manual for the machine that is intended for use by software developers (See Fig 1 step 2113 and 0036), and b) the content of an internal register of the machine that is explicitly identified in an instruction manual for the machine that is intended for use by software developers but is stored in a format or location that is not explicitly identified in an instruction manual for the machine that is intended for use by software developers(See Fig 1 step 2113 and 0036).

33. As per claim 33: Hashimoto discloses further comprising storing the recovered private data in a private storage of the machine (See 0036-0037).

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fikremariam Yalew whose telephone number is 5712723852. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moazzami Nasser,can be reached on 5712738300. The fax phone number for the organization where this application or proceeding is assigned is 571-272-4195.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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